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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,024	04/20/2004	Aaron Ferrucci	ALTRP112/A1251	5974

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/829,024	FERRUCCI ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/20/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a Non-Final Action in response to the instant U.S. Application filed 04/20/2004. Claims 1-30 are pending and presently under examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1-3, 5-15, 17-24 and 26-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Williams (U.S. Patent No. 5,898,895) issued: April 27, 1999.

Regarding independent Claims 1, 28, Williams discloses a method and means for testing arbitrator logic 124 or bus interface logic 122 of the bridge 108, Figure 3, comprising:

Receiving a read request on line 134 at a secondary component (downlink module 116) from a primary component (uplink module 118), which is coupled, to the arbitrator logic 124 through a read request control line 126, Figures 3 and 4.

Determining a pseudo-random delay, using variable read acknowledge logic 138 for determining the time delay of the read acknowledge signal, which is located in the downlink module 116, prior to responding to the read request with the read acknowledge signal on line 136.

Using variable read acknowledge logic 138 to pseudo-randomly delay the response of the acknowledge signal on line 136.

A pulse generator 170 generates plurality of delay pulses corresponding to a "pseudo-random delay", shown as DELAYS 1-4, since the delay requirement can be randomly selected depending on the clock speed.

Regarding independent Claim 13, Williams discloses a system interface, Figure 3, comprising:

An I/O interface bridge 108 connected to the I/O bus 106 to allow the I/O devices to communicate with the memory system, the interface bridge is configured to communicate with the uplink module 118 through the read request control line 126.

A delay mechanism, such as a variable read acknowledge logic 138 for determining the time delay of the read acknowledge signal, which is located in the downlink module 116, prior to responding to the read request with the read acknowledge signal on line 136, and using variable read acknowledge logic 138 to pseudo-randomly delay the response of the acknowledge signal on line 136.

Regarding independent Claim 21, Williams discloses a system comprising:

A plurality of primary (uplink module 118) and secondary (downlink module 116) components for receiving a read request on line 134 at a secondary component (downlink module 116) from a primary component (uplink module 118) which is coupled to the arbitrator logic 124 through a read request control line 126, Figures 3 and 4.

An arbitrator logic 124 from making bus requests simultaneously, which is coupled as shown in Figure 3. Various different arbitration techniques can be used, including fixed priority schemes, round-robin priority schemes and other schemes.

The (downlink module 116) including a pseudo-random delay, using variable read acknowledge logic 138 for determining the time delay of the read acknowledge signal, which is located in the downlink module 116, prior to responding to the read request with the read acknowledge signal on line 136.

Regarding Claims 2, 3, 5-6, 9-12, 14, 15, 17-20, 22-24, 26, 27, 29, 30, Williams discloses variable read acknowledge logic 138, which accepts one or more clock signal pulses from pulse generator 170, and generating the read acknowledge signal on line 136. As shown in Figure 7, the pulse generator 170 generates the delay signals labeled phase-A, B, C and D, on lines 180, 182, 184 and 186 respectively. In order to provide a variable delay for the return of the read acknowledge signal on line 136, a plurality of delay pulses are provided, one of which is selected by the variable read acknowledge logic 138 and transmitted to uplink module 118 via line 136.

Regarding Claims 7, 8, Williams discloses arbitrator logic 124 from making bus requests simultaneously. Various different arbitration techniques can be used, including fixed priority schemes, round-robin priority schemes and other schemes.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 16 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams (U.S. Patent No. 5,898,895) in view of Malek (U.S. Patent No. 5,086,467).

Regarding Claim 4, Williams does not explicitly disclose a Linear Feed Back Shift register (LFSR) as delay mechanism.

However, in analogous art, Malek (US 5,086,467) discloses a secure communication system including a pseudo-random sequence itself, which is ideally suited for determining both the duration and the inter-transmission delays by using the output of the LFSR to seed random variable generators, one of which may be used to select the duration of any dummy traffic transmission, and the other of which may be used to determine the inter-transmission delay, or time between transmissions, (see Malek, Summary of the Invention and Figure 3). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate an LFSR as taught by Malek in the variable acknowledge logic of Williams, for the purpose of generating a pseudo-random delay, since an LFSR is ideally suited for determining time delays.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAMES C KERVEROS
Examiner
Art Unit 2138

5/5/06

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Office Action: Non-Final Rejection